REMARKS

Claims 1-12, and 14-16 are pending. Claims 2 and 3 have been cancelled. Claims 1, 12, and 14-16 have been amended. No new matter has been added by way of this amendment. Reconsideration of the application is requested.

Claim 14 stands rejected under 35 U.S.C. §112. 2nd ¶, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. According to the Examiner, claim 14 depends from cancelled claim 13. in response to this rejection, Applicant has amended claims 14 such that it now depends from claim 12. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

Claims 1, 4, 7, and 8 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,317,820 to *Shiell* et al., while claims 5, 6, 9-12, 14, and 15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the same reference in view of U.S. Patent No. 5,761,470 to *Yoshida*. In addition, claim 16 stands rejected under 35 U.S.C. §102(b) as being anticipated by the *Yoshida* patent. In response to these several grounds of rejection, Applicant has amended independent claims 1, 12, and 15 to emphasize those features of the invention that distinguish it from the cited reference. Accordingly, for the reasons set forth hereafter, Applicant respectfully submits that all claims of record now distinguish over the cited references.

Independent claims 1, 12, and 15 have been amended to recite the "decode unit being operable to control the first and second channels such that, when the decode unit detects that the instruction defines two independent operations, it is operable to control the first channel

to implement one of those operations and the second channel to implement the other of those operations, whereby the first and second channels execute their respective independent operations simultaneously." This limitation is also set forth in method claim 8, which recites the "instruction defines two independent operations, supplying one of the operations to the first processing channel and the other of the operations to the second processing channel whereby the operations are executed simultaneously."

With reference to Fig. 2a and Fig. 2b, the present claimed invention is directed to a computer system employing an instruction stream comprising a sequence of instructions of the same "predetermined length". Among these instructions, there are instructions which define single operations and instructions which define dual operations. The instruction format and decode unit are configured such that the claimed computer system can execute single operations or dual operations, each employing the resources of the computer differently, based on the identification bits within the instruction (see ID1 and ID2 in Figs. 2a and 2b). As a consequence, only one decode unit and one set of instructions bit per predetermined bit length is needed. This drastically simplifies the fetch decode and instruction semantics required to achieve a given level of performance, while retaining the capability of selecting between levels of instruction parallelism. This novel feature of the invention is reflect in all of the independent claims and is not disclosed in any of the presently cited prior art documents.

U.S. Patent No. 6,317,820 to *Shiell* et al. relates to a computer system having CPU 200 having a dual ported program memory 105, an instruction despatch/decode unit 115A, B, A-side and B side execution channels, each comprising a register unit S, an integer unit L, a multiplier accumulator unit M and a data load store unit D (see Fig. 2). The data is supplied from a data memory 160 via the register files for side A and side B in a conventionally known

manner. *Shiell* uses the term very long instruction word (VILW). Here, the very long instruction word merely comprises a block of 8 single instructions that are simultaneously transferred between certain upstream components to speed up fetching processes (see col. 3, lines 65-66). Accordingly, this architecture can fetch one VILW (or 8 individual instructions) per cycle and supply a maximum of 4 instructions to each of the A and B sides, assuming that each requires a separate functional unit per cycle.

The system disclosed in *Shiell* et al. is directed to supplying additional (duplicate) components so that the computer can support both a first mode of operation and a second mode of operation. In the first mode, the data processor executes a single instruction stream. In the second mode, the data processor executes two independent program instruction streams simultaneously. To do this, fetch/decode circuitry is divided into two parts 115A and 115B each serving a separate side (see for example col. 4, lines 35-44). In addition, fetch program counter and control units 110A and 110B are each used to fetch a half packet of instructions, (1/2 of a VLIW eight instruction packet) from program memory 105 (which is now dual ported), into respective Instruction Dispatch/Decode units 115A and 115B (see col. 4, line 66 thru col. 5, line 4). This permits the CPU to process two instruction streams (each corresponding to half of the VILW 8 instruction packet) simultaneously. However, *Sheill* et al. fail to teach the limitations the "decode unit being operable to control the first and second channels such that, when the decode unit detects that the instruction defines two independent operations, it is operable to control the first channel to implement one of those operations and the second channel to implement the other of those operations, whereby the first and second channels execute their respective independent operations simultaneously," and the "instruction defines two independent operations, supplying one of the operations to the first processing channel and the other of the

operations to the second processing channel whereby the operations are executed simultaneously," as set forth in amended independent claims 1, 12 and 15, and method claim 8, respectively. Here the decision of whether to implement parallel processing is based on the bits ID1 and ID2 that are contained within the instruction itself.

In the *Sheill* et al. patent, the instructions themselves do not indicated whether parallel processing should be used, i.e., no signalling from within the instruction is used in this system. Rather, *Sheill* et al. requires separate control units 110A and 110B to produce the instruction streaming as taught therein. It follows that there is simply no ability for a single fixed length instruction to be flexible as to whether its a single or multiple operation. Hence, it is impossible to conclude that the *Shiell* et al. patent teaches or suggests the limitations set forth in amended independent claims 1, 12, and 15, and method claim 8.

U.S. Patent No. 5,761,470 to *Yoshida* discloses a data processor that achieves an improved instruction code efficiency, in which the necessity of specifying null operations is reduced by flexibly controlling the number and the order of operations. According to this patent, this is accomplished by using a format field which specifies the number of the operation fields and the order of the operations (se col. 2, lines 1-7). However, this patent fails to cure the deficiency of the *Sheill* et al. patent; in that *Yoshida* also fails to teach the "decode unit being operable to control the first and second channels such that, when the decode unit detects that the instruction defines two independent operations, it is operable to control the first channel to implement one of those operations and the second channel to implement the other of those operations, whereby the first and second channels execute their respective independent operations simultaneously," and the "instruction defines two independent operations, supplying

one of the operations to the first processing channel and the other of the operations to the second processing channel whereby the operations are executed simultaneously."

Set forth on page 9, paragraph 24 is the statement that:

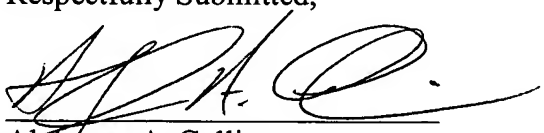
> "Shiell et al. have not taught the instructions containing a set of designated bits at predetermined bit locations within said bit length and said decoding step including reading the values of said designated bits to determine steps a) and b) above. However Yoshida has taught instructions containing a set of designated bits at predetermined bit locations within said bit length (Figure 25, elements 505 and 506) and said decoding step including reading the values of said designated bits to determine steps a) (Figure 25, Figure 26, FM) and b) (column 7, lines 1-36, column 19, line 65 - column 20, line 4) above. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instructions of Shiell et al. contain a set of designated bits at predetermined bit locations within said bit length, as taught by Yoshida, in order to easily determine whether the bit length defines a single operation or two independent operations. Having the designated bits at predetermined bit locations in the instruction itself would eliminate the need to have a separate instruction (Shiell et al., column 2, lines 53-55) preceding the instruction in order to set up the channels for execution."

With respect to the foregoing, Applicant respectfully asserts that although *Yoshida* discloses bits within an instruction, it is only for use by a single channel processor. It follows that this reference also fails to teach two channels that operate either independently or in cooperation with each other. This is clearly shown in Fig. 23 and described in col. 18, lines 719. Applicant respectfully asserts that having two channels that operate either independently or in cooperation, as signalled by instructions bits in a single instruction, permits greater processing flexibility, i.e., the performance of parallel arithmetic operations. Accordingly, neither *Shiell* et al. nor *Yoshida*, neither individually nor in combination, teach or suggest the invention as claimed, and hence the rejection of the independent claims independent claims 1, 8, 12, and 15 should be reconsidered and withdrawn.

In light of the patentability of independent claims 1, 8, 12, and 15, for the reasons above, dependent claims 3-7, 9-11, 14, and 16 are patentable over the prior art.

In view of the foregoing amendments and remarks, this application should be in condition for allowance. Early passage of this case to issue is respectfully requested. However, if there are any questions regarding this Response, or the application in general, a telephone call to the undersigned would be appreciated since this would expedite the prosecution of the application for all concerned.

Respectfully Submitted,



Alphonso A. Collins
Reg. No. 43,559
Attorney for Applicant

DARBY & DARBY P.C.
805 Third Avenue
New York, New York 10022
(212) 527-7700